



(1/11)

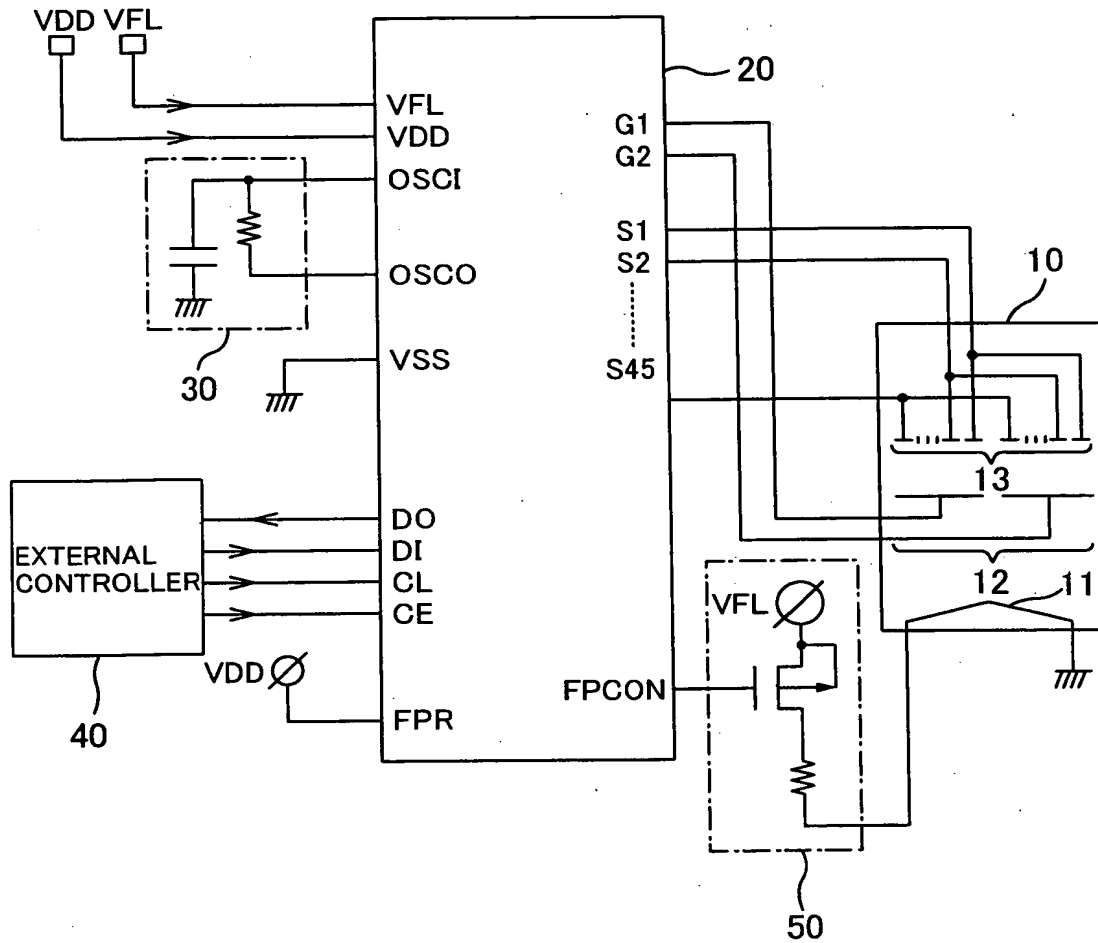
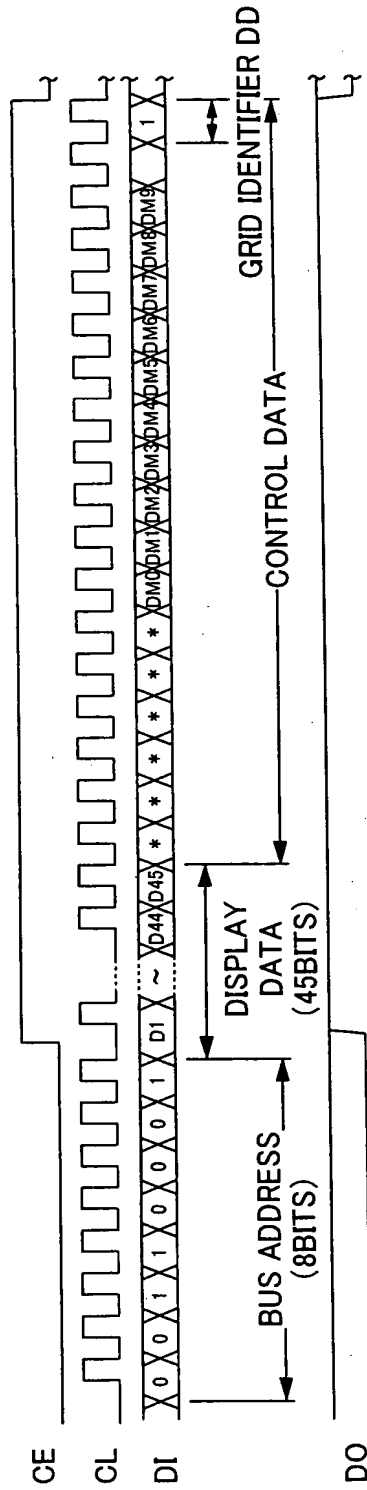


FIG.1

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(a) G1 SEQUENCE



(b) G2 SEQUENCE

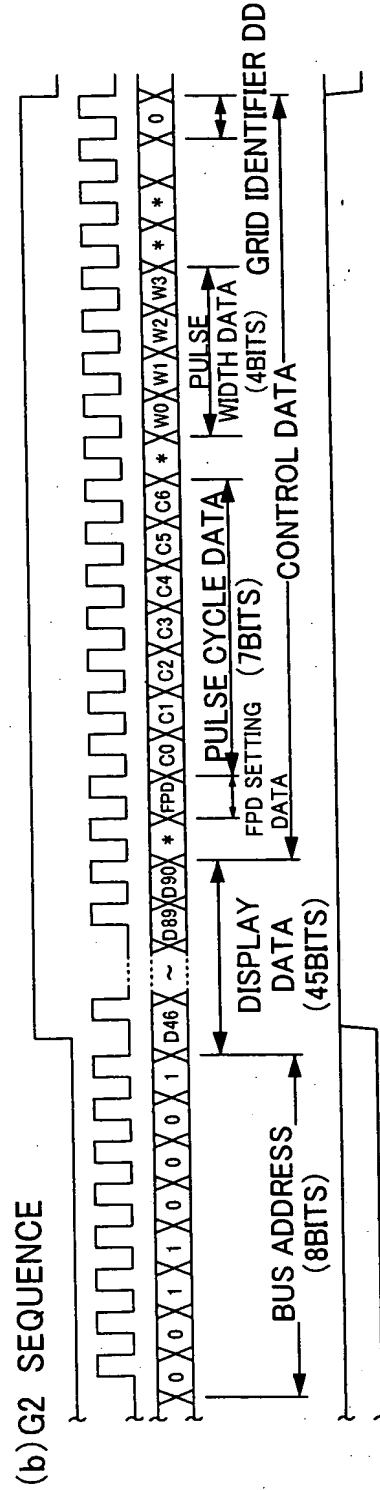
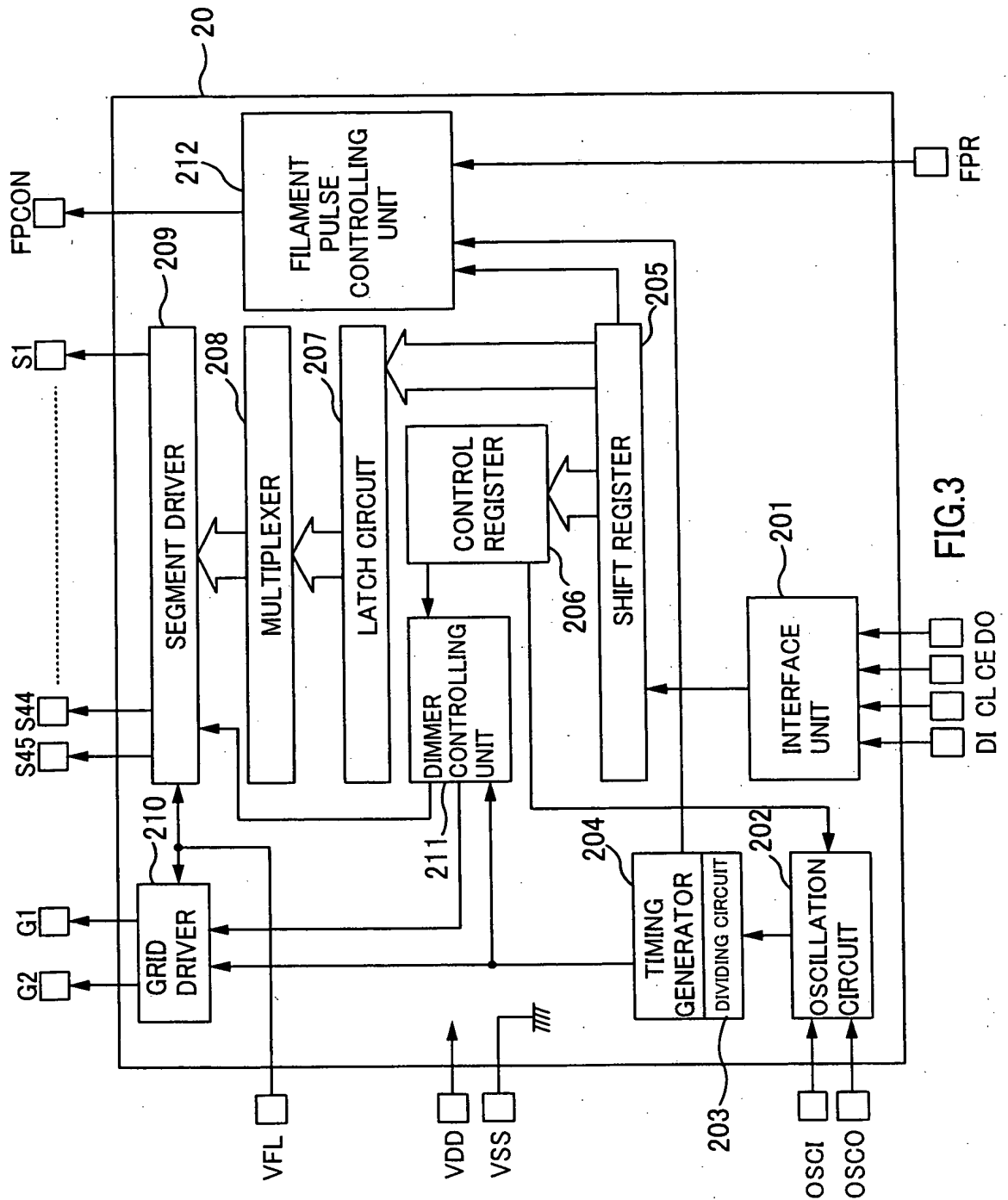


FIG.2

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(4/11)

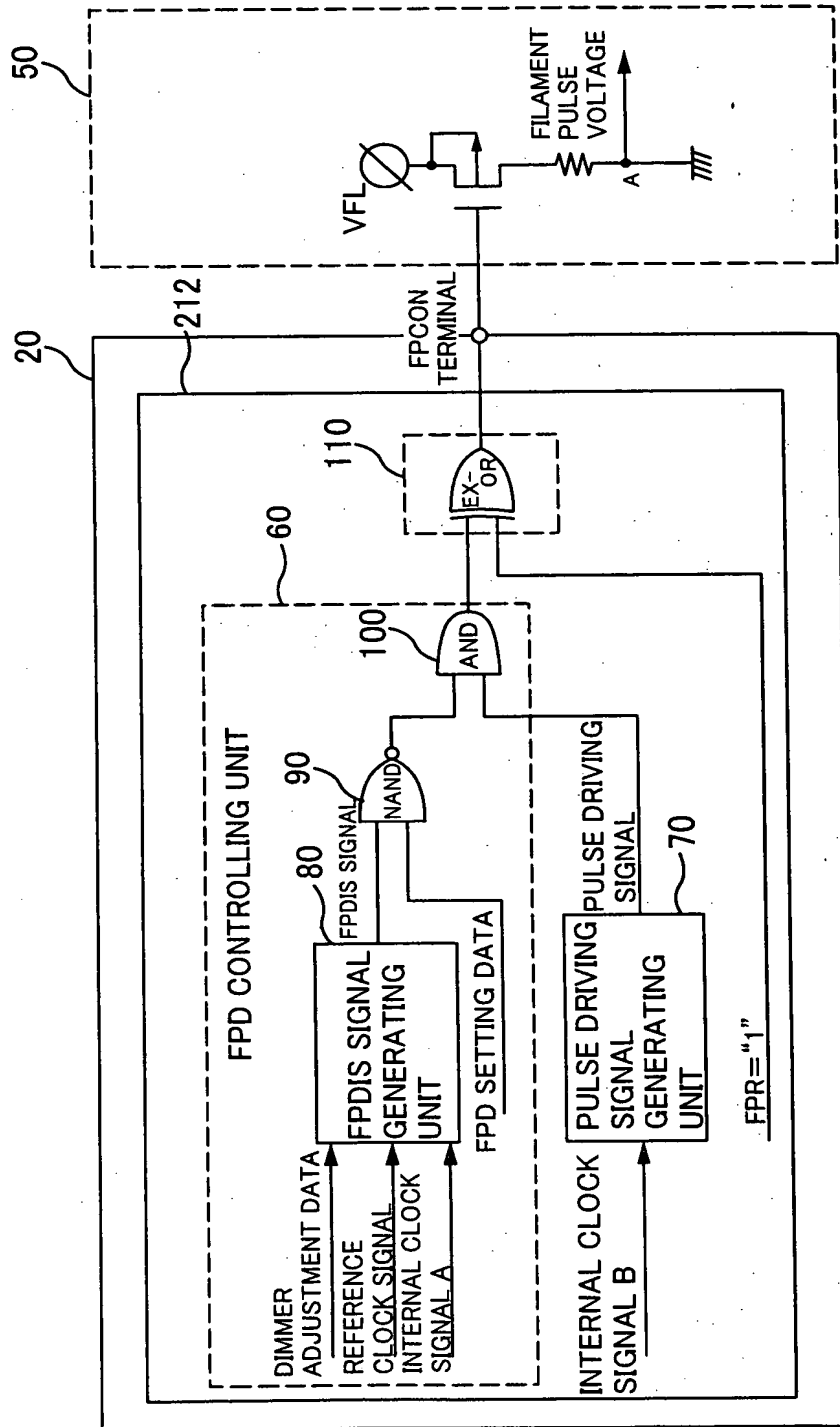


FIG.4

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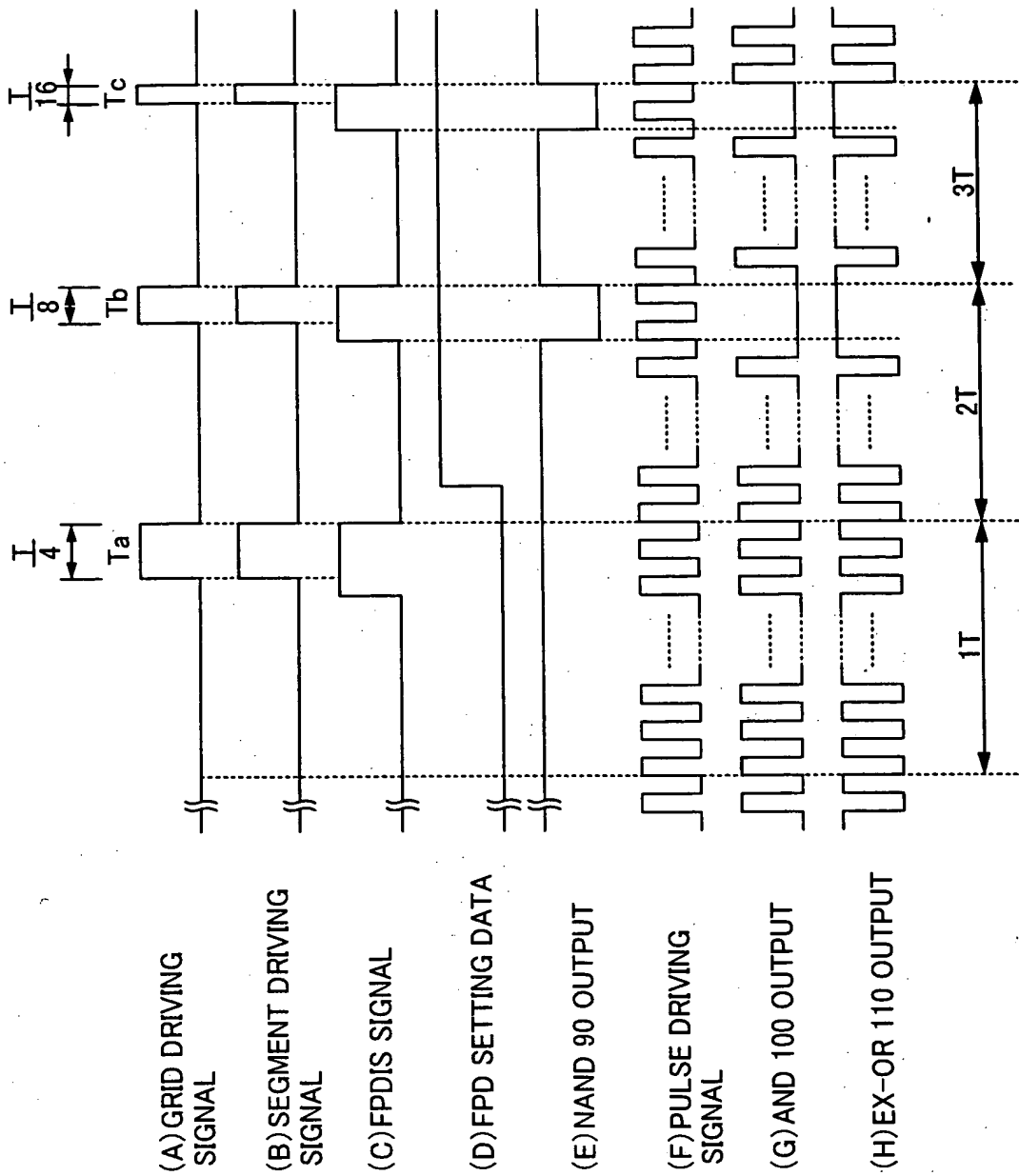


FIG.5

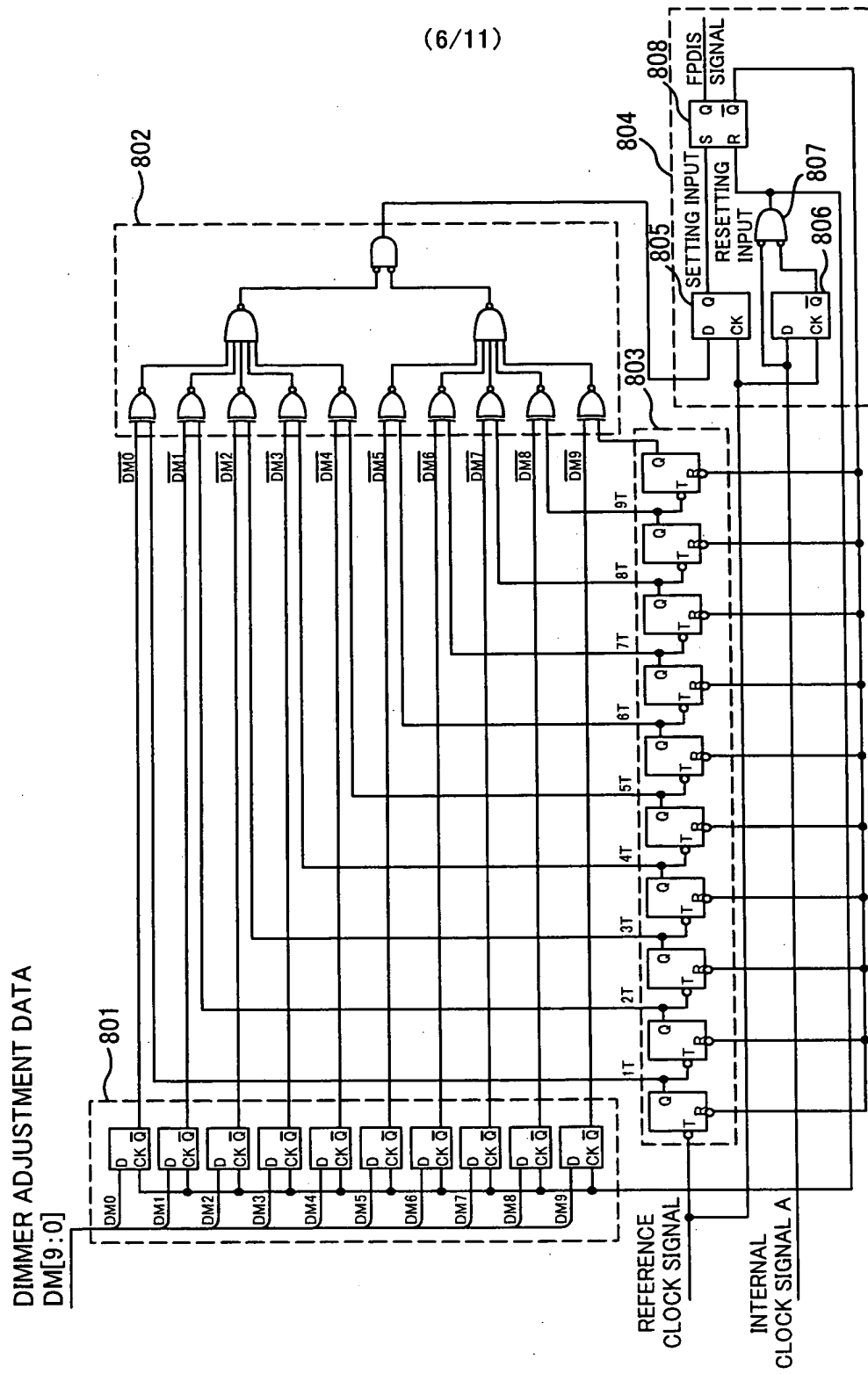
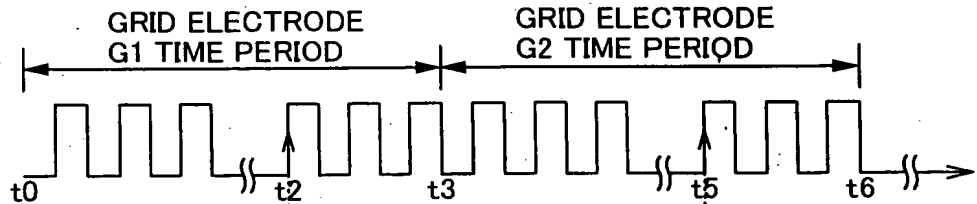


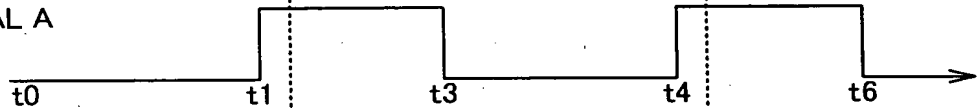
FIG.6

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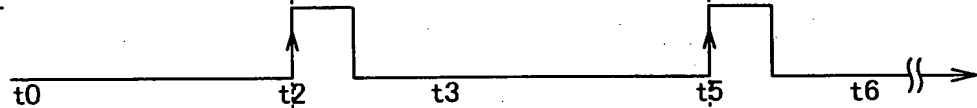
(A) REFERENCE CLOCK SIGNAL



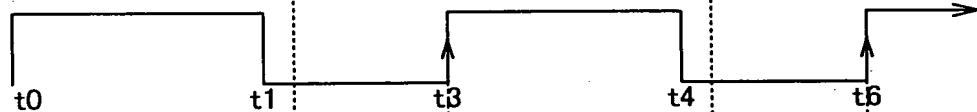
(B) INTERNAL CLOCK SIGNAL A



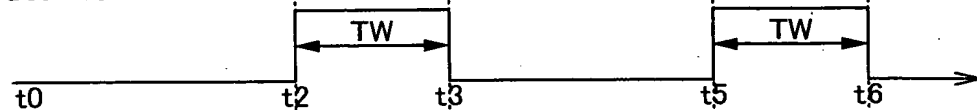
(C) RS-FF SETTING INPUT



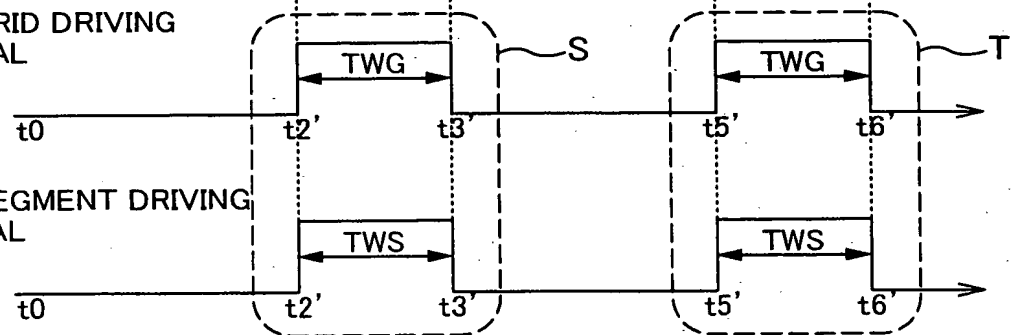
(D) RS-FF RESETING INPUT



(E) FPDIS SIGNAL



(F) GRID DRIVING SIGNAL



(G) SEGMENT DRIVING SIGNAL

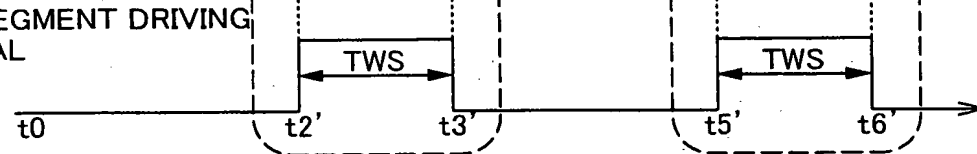


FIG.7

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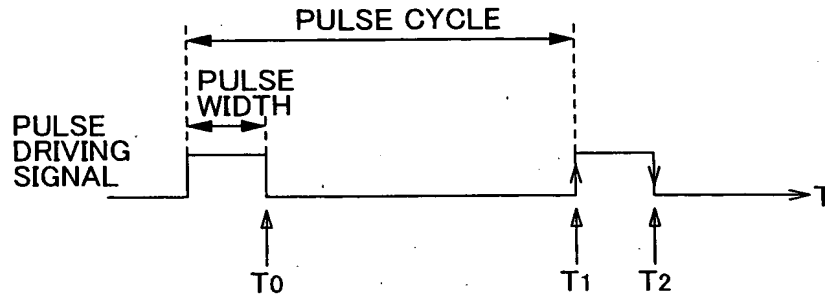


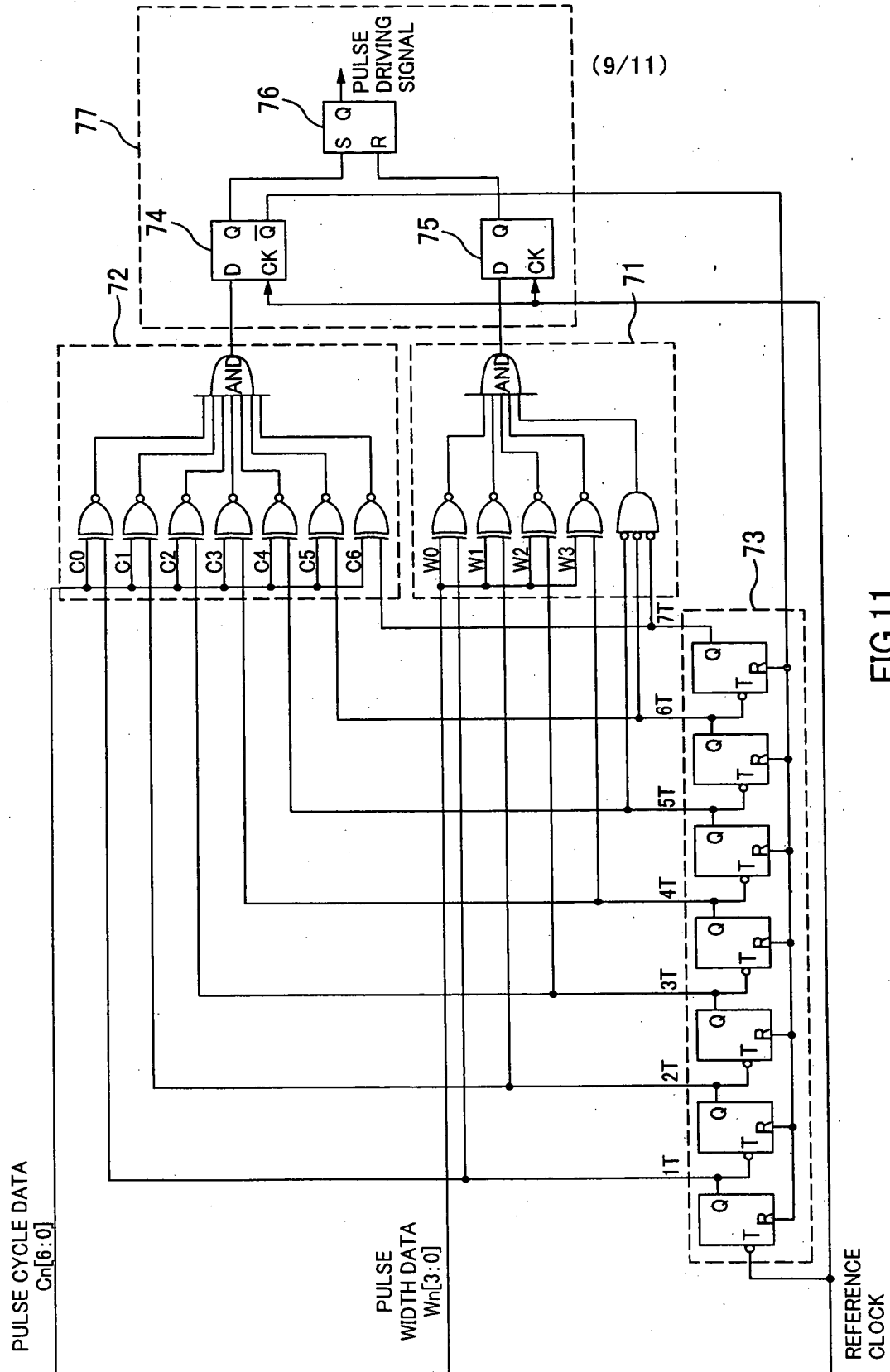
FIG.8

W3	W2	W1	W0	VALUE SET FOR W _n	FPC PULSE WIDTH
0	0	0	0	—	—
0	0	0	1	3	3/fosc
0	0	1	0	4	4/fosc
~					~
0	1	1	0	8	8/fosc
~					~
1	1	1	0	16	16/fosc
1	1	1	1	17	17/fosc

FIG.9

C6	C5	C4	C3	C2	C1	C0	VALUE SET FOR C _n	FPC PULSE CYCLE
0	0	0	0	0	0	0	—	—
0	0	0	0	0	0	1	—	—
0	0	0	0	0	1	0	4	4/fosc
0	0	0	0	0	1	1	5	5/fosc
~								~
1	0	0	0	1	1	0	72	72/fosc
~								~
1	1	1	1	1	1	0	128	128/fosc
1	1	1	1	1	1	1	129	129/fosc

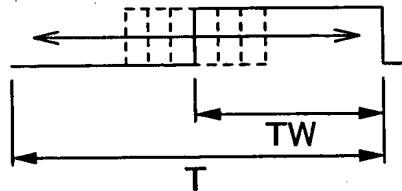
FIG.10



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DIMMER ADJUSTMENT DATA										DIMMER VALUE(TW/T)
DM9	DM8	DM7	DM6	DM5	DM4	DM3	DM2	DM1	DM0	
0	0	0	0	0	0	0	0	0	0	0/1024
0	0	0	0	0	0	0	0	0	1	1/1024
0	0	0	0	0	0	0	0	1	0	2/1024
										}
1	1	1	1	1	1	1	1	0	0	1020/1024
1	1	1	1	1	1	1	1	0	1	1021/1024
1	1	1	1	1	1	1	1	1	0	1022/1024
1	1	1	1	1	1	1	1	1	1	IMPOSSIBLE TO SET

(a)



(b)

FIG.12

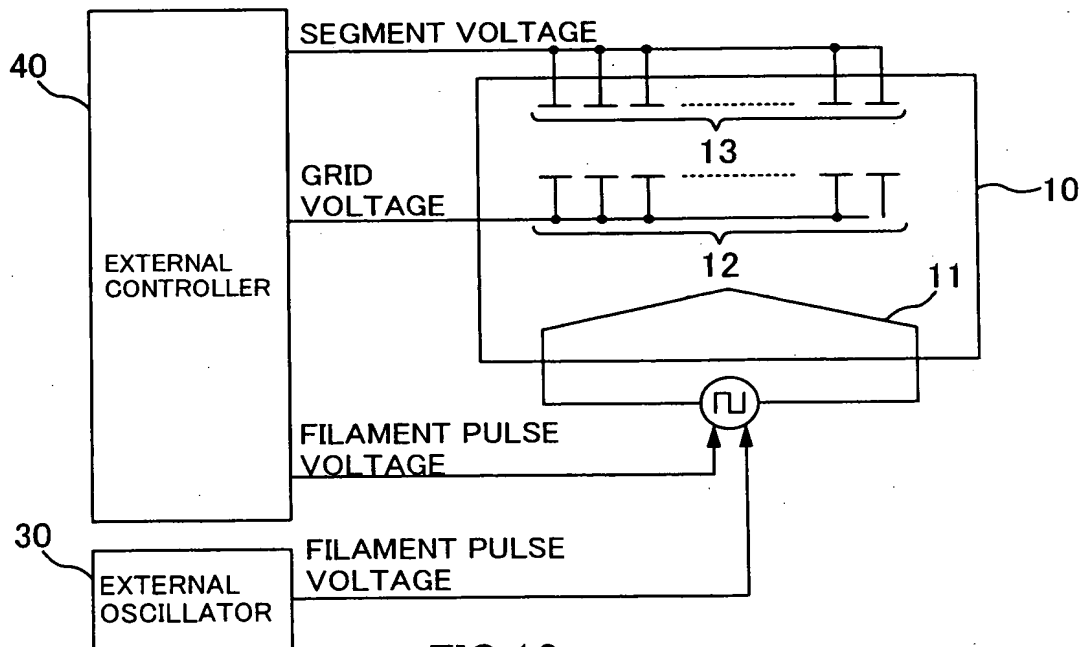


FIG.13

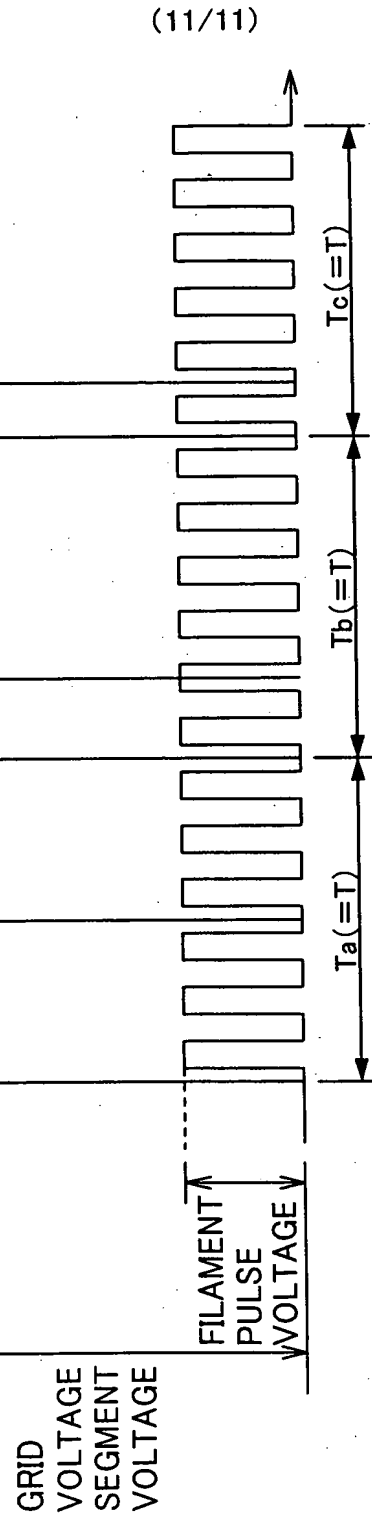


FIG.14